WHAT IS CLAIMED IS:

1. A method for manufacturing a semiconductor component, comprising:
providing a semiconductor substrate having a major surface;
forming a dielectric material over the major surface;
forming an opening in the dielectric material, the opening having sidewalls;
lining the opening with a barrier layer; and
forming a multi-metal seed layer on the barrier layer.

2. The method of claim 1, wherein forming the multi-metal seed layer comprises:
forming a first metal oxide layer on the barrier layer; and
forming a second metal oxide layer on the first metal oxide layer.

3. The method of claim 2, wherein forming the multi-metal seed layer further includes reducing the first and second metal oxide layers.

4. The method of claim 3, wherein reducing the first and second metal oxide layers includes heating the first and second metal oxide layers to a temperature of at least 150 degrees Celsius.

5. The method of claim 2, wherein forming the first metal oxide layer includes using atomic layer deposition to form the first metal oxide layer.

6. The method of claim 5, wherein forming the second metal oxide layer includes using atomic layer deposition to form the second metal oxide layer.

7. The method of claim 2, wherein forming the first metal oxide layer includes using a metal oxide selected from the group of metal oxides consisting of copper oxide, tin oxide, silver oxide, and zinc oxide.

8. The method of claim 2, wherein forming the second metal oxide layer includes using a metal oxide selected from the group of metal oxides consisting of copper oxide, tin oxide, silver oxide, and zinc oxide.

9. The method of claim 2, wherein forming the multi-metal seed layer further comprises forming a third metal oxide layer on the second metal oxide layer.

10. The method of claim 9, wherein first metal oxide layer comprises copper oxide, the second metal oxide layer comprises tin oxide layer, and the third metal oxide layer comprises copper oxide.

11. The method of claim 1, further including forming a layer of copper on the multi-metal seed layer.

12. The method of claim 1, wherein forming the multi-metal seed layer includes using a metal selected from the group of metals consisting of copper, tin, silver, and zinc.

13. The method of claim 1, wherein forming the multi-metal seed layer includes forming the multi-metal seed layer to have a thickness of less than approximately 300 Angstroms.

14. An intermediate structure suitable for use in a semiconductor component, comprising:

a substrate having a surface;

a dielectric layer disposed over the surface, the dielectric layer having an opening;

a barrier layer lining the opening; and

a precursor seed material disposed on the barrier layer, wherein the precursor seed material includes at least one metal oxide layer.

15. The intermediate structure of claim 14, wherein the at least one metal oxide layer includes:

a first metal oxide layer disposed on the barrier layer; and

a second metal oxide layer disposed on the first metal oxide layer.

16. The intermediate structure of claim 15, wherein the at least one metal oxide layer includes a third metal oxide layer disposed on the second metal oxide layer.

17. The intermediate structure of claim 16, wherein the first metal oxide layer comprises copper oxide, the second metal oxide layer comprises tin oxide, and the third metal oxide layer comprises copper oxide.

18. The intermediate structure of claim 15, wherein the first metal oxide layer comprises copper oxide and the second metal oxide layer comprises tin oxide.

19. The intermediate structure of claim 14, wherein the at least one metal oxide layer comprises a metal oxide selected from the group of metal oxides consisting of copper oxide, tin oxide, silver oxide, and zinc oxide.

20. A semiconductor component, comprising:
a dielectric layer having an opening;
a barrier layer lining the opening; and
a multi-metal seed layer disposed on the barrier layer.

21. The semiconductor component of claim 20, further including an electrically conductive material disposed on the multi-metal seed layer.

22. The semiconductor component of claim 21, wherein the electrically conductive material comprises copper.

23. The semiconductor component of claim 20, wherein the multi-metal seed layer comprises copper and tin.

24. The semiconductor component of claim 20, wherein the multi-metal seed layer comprises at least two metals selected from the group of metals consisting of copper, tin, silver, and zinc.

25. The semiconductor component of claim 20, wherein the multi-metal seed layer has a thickness of less than approximately 300 Angstroms.

26. The semiconductor component of claim 20, wherein the multi-metal seed layer has a concentration of tin ranging from approximately 0.1 atomic percent to approximately 10 atomic percent.